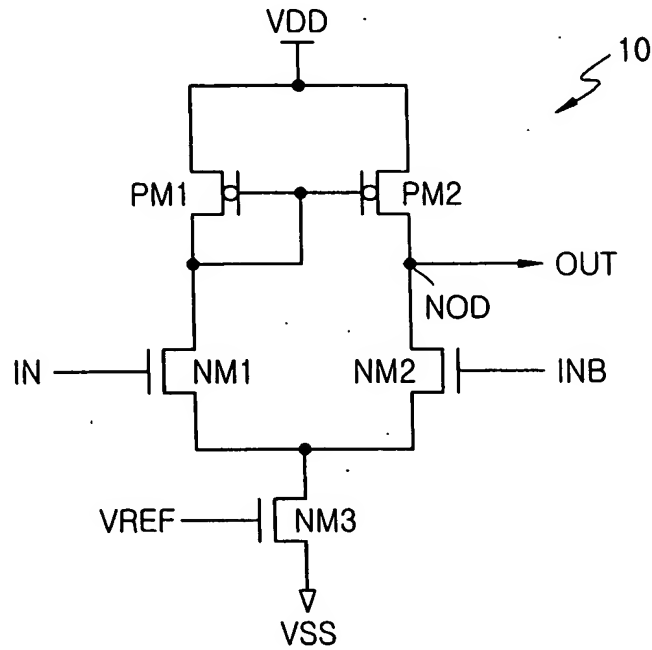


AMPLIFIER CIRCUIT WITH OUTPUT DELAY SELECTIVELY CHANGED ACCORDING TO COMMON
MODE VOLTAGE LEVEL, ASSOCIATED REPLICA DELAY CIRCUIT AND INTERNAL CLOCK
GENERATOR

Application No. NEW - Docket No. SEC.1158

Inventor: Won-ki PARK

FIG. 1 (PRIOR ART)



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FIG. 3A (PRIOR ART)

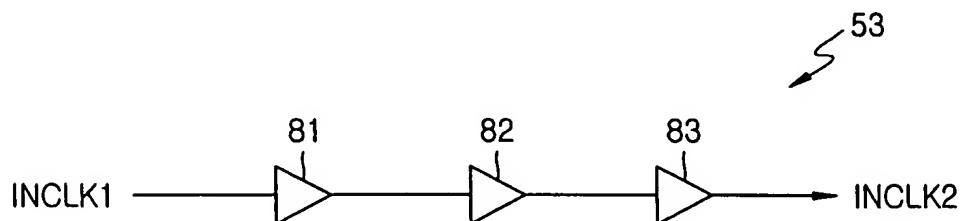
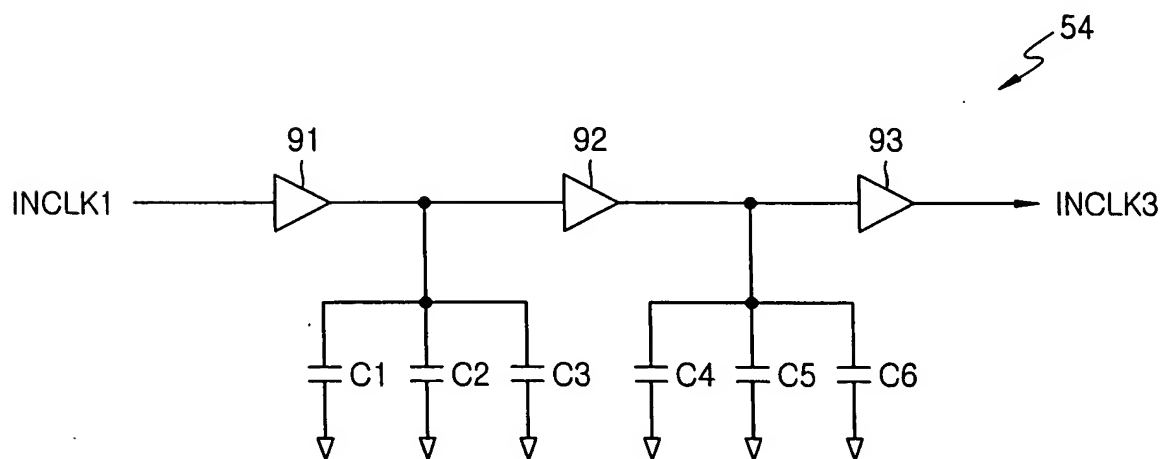


FIG. 3B (PRIOR ART)



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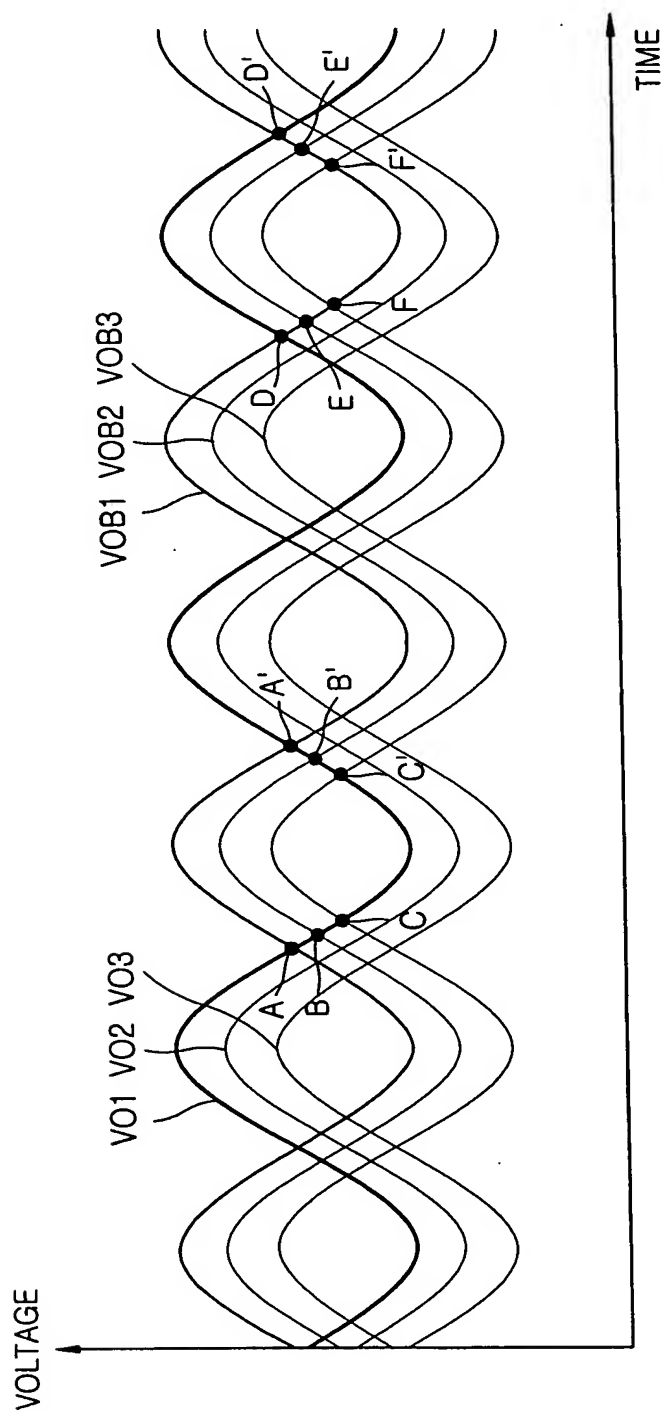
[illegible]

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FIG. 5



AMPLIFIER CIRCUIT WITH OUTPUT DELAY SELECTIVELY CHANGED ACCORDING TO COMMON
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FIG. 6A

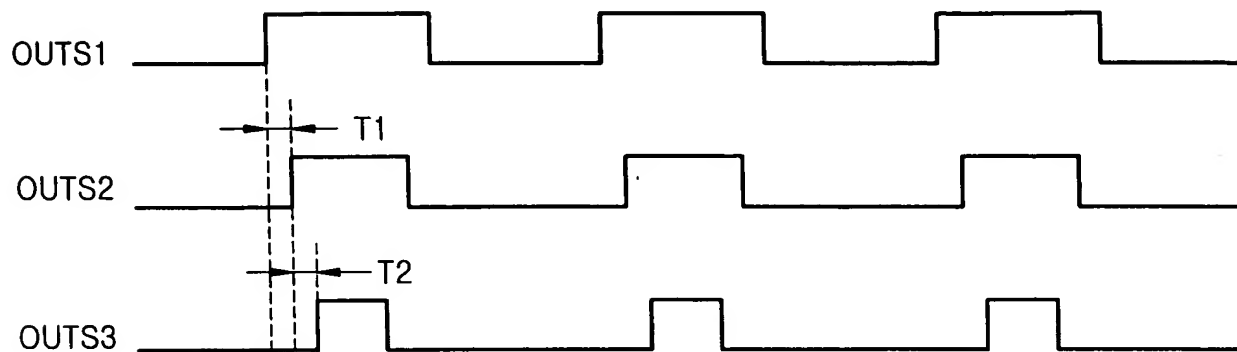
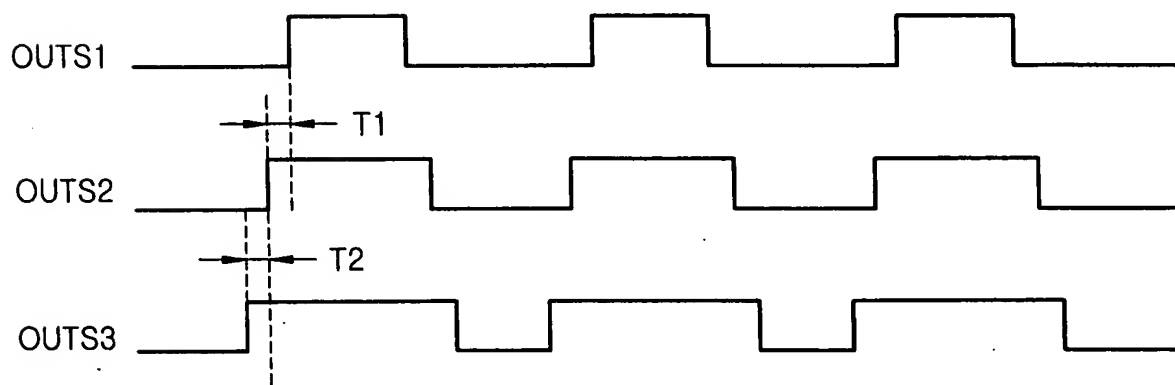


FIG. 6B



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graph LR
    CLK_EX[CLK_EX] --> 210[VARIABLE DELAY CIRCUIT]
    210 -- CLK_IN1 --> 220[BUFFER CIRCUIT]
    220 -- CLK_IN2 --> 301[INTERNAL OUTPUT CIRCUIT]
    301 --> 302[OUTPUT DRIVER]
    302 -- DATA --> DATA_OUT[DATA]
    301 --> 240[PHASE DETECTOR]
    240 -- CLK_RE --> 230[REPLICA DELAY CIRCUIT]
    230 --> 210
    250[CONTROL SIGNAL GENERATOR] -- VCTL1 --> 230
    250 -- ~VCTL6 --> 230
    subgraph 200 [200]
        210
        220
        230
        240
    end
    subgraph 300 [300]
        301
        302
    end

```

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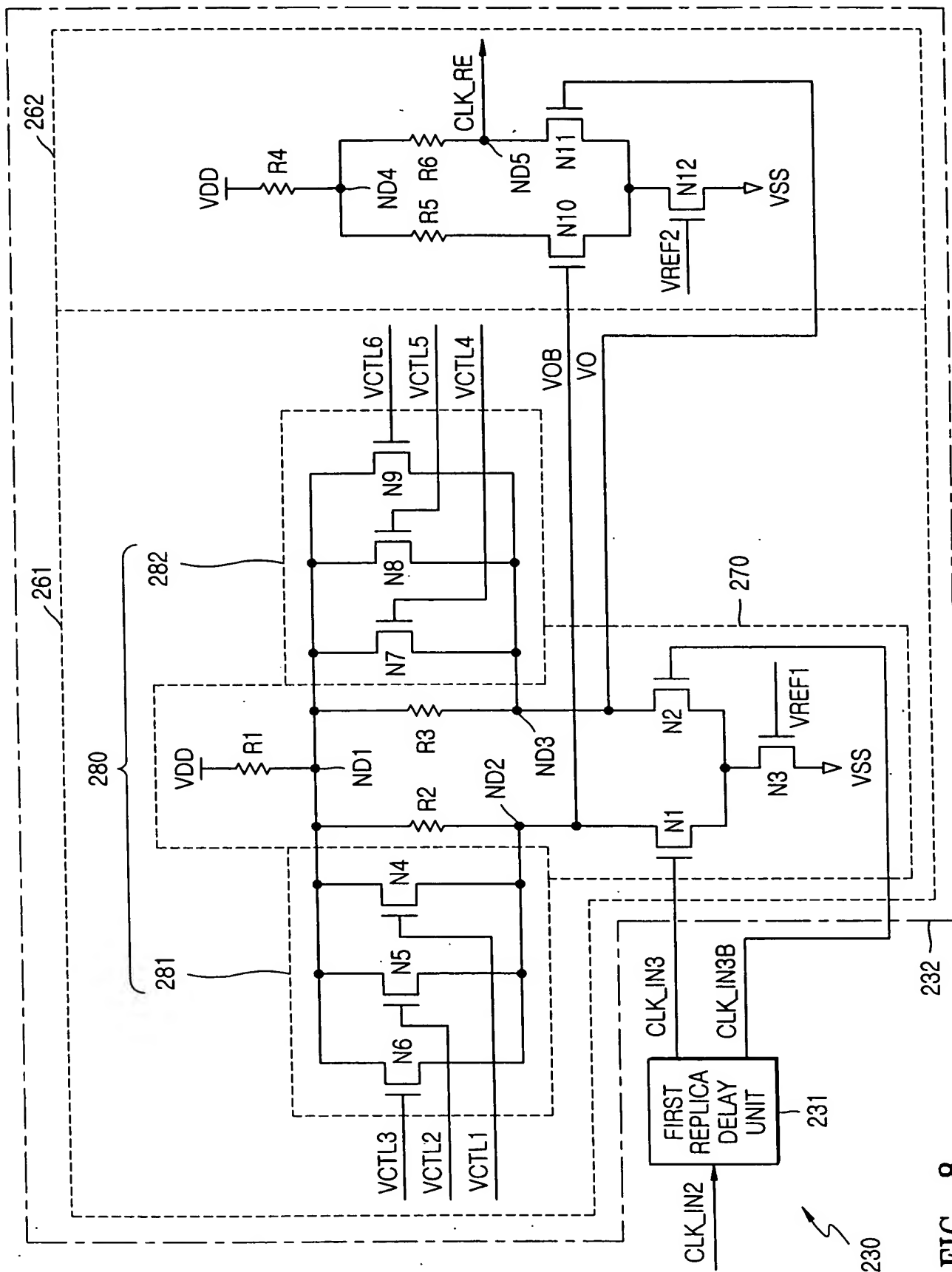


FIG. 8